

November 20, 2009

Today in 1985 – Microsoft Windows 1.0 is released.

[SEMATECH Names IBM Exec as New CEO](#)
[Semiconductor Revenue to Rebound in 2010](#)
[CNSE Presents First-Ever 'Nano in the Mall' Program](#)
[Thin Film's Solar Share to Double by 2013](#)
[SEMATECH EUV Program making Progress](#)
[Toppan, Casio to Form OLED Display Venture](#)
[Nanotech Product of the Week](#)

The SEMATECH semiconductor research consortium has named IBM executive Daniel Armbrust as its new president and CEO, effective immediately. Armbrust succeeds Michael Polcari, SEMATECH's CEO for the past six years. Polcari, also a veteran IBM executive, remains as chairman of the board. Polcari said SEMATECH's boards chose Armbrust based on his track record of leadership and execution in developing leading edge chip manufacturing technologies, directing factory operations and managing complex alliances.

"Dan came to our attention because of his proven ability to lead top performing teams, his strong credentials in both R&D and manufacturing, and his experience in driving strategic alliances." Polcari said in a press release. Armbrust, a 25 year IBM employee, previously was vice president of 300 millimeter chip operations for Big Blue, where he was responsible for that company's most advanced factory and research complex in East Fishkill, N.Y. IBM and its various technology alliance partners all have researchers at the complex.



The appointment of Armbrust, 47, came as somewhat of a surprise because it was not known -- at least outside the semiconductor industry -- that a search was under way for Polcari's replacement. But Armbrust is well known at the UAAlbany NanoCollege and its \$5 billion Albany NanoTech Complex, where IBM has a major presence.

"With top-flight credentials that include leadership roles in support of IBM's global nanoelectronics research, manufacturing and strategic alliances, Dan Armbrust is uniquely qualified to lead Sematech during this exciting time in the organization's history," said Alain Kaloyeros, the CEO of the NanoCollege. "We look forward to working closely with Dan to further build the successful partnership."

The 22-year-old research consortium is headquartered in Austin, but it has substantial and growing operations Albany, N.Y., where it has research operations located CNSE's Albany NanoTech Complex. The consortium is considered to be a leading player in collaborative research aimed at developing next-generation chips and equipment and in running existing semiconductor factories more efficiently.

[Return to Top](#)

Gartner Inc has once again revised its 2009 semiconductor sales forecast upward. According to the market research company, semiconductor revenue is on pace to total \$226 billion in 2009, compared to 2008 revenue of \$255 billion. The expected drop is less than half of the company's original projections for the year's decline. The company had estimated in Q1 that revenue could fall more than 24%. In Q4, that projection was revised to a 22.4% drop. And Gartner in Q3 revised its estimated 2009 semiconductor revenue decline to 17.1%.

Crediting inventory replenishment, government stimulus packages, price elasticity on consumer products, and "amazingly strong" consumer high-tech spending, Gartner reported that the semiconductor market's recovery is well under way and that its outlook continues to improve as semiconductor suppliers post outstanding quarterly results. Gartner said Q2 showed close to 17% growth for the industry, while Q3 experienced almost 20% growth. Company guidances for Q4 are also well above the seasonal norm, signaling continued expansion of a strong semiconductor industry recovery, Gartner said.

Looking to 2010, [Gartner](#) said semiconductor revenue is expected to bounce back to the same revenue level as 2008 at \$255 billion, a 13% increase from 2009. "The most significant changes for the semiconductor industry came from application-specific standard products (ASSPs), memory, and compute microprocessors, as all three products benefited from a strengthening PC market," said Bryan Lewis, research VP at Gartner, in a statement this morning. "ASSPs and memory, primarily NAND flash, also benefited from an improved outlook for cell phones. "The revenue forecast for the commodity memory market — DRAM and NAND flash — has improved because of the stronger demand outlook, which means that pricing has strengthened more than previously forecast," Lewis said.



According to Gartner, PCs are the single largest application driving the semiconductor rebound. The company said PC unit growth projections dramatically improved from double-digit declines at the start of 2009 to a current low-single-digit positive outlook, allowing for lesser declines for MPUs and DRAM. "Both device types experienced lower revenue declines than the industry average, and DRAM began to be profitable for some vendors in the third quarter of 2009 after almost three years of losses," Lewis said. "While most of the news has been positive to date, recent channel checks in Taiwan indicate there is concern that PC orders are slowing earlier than the seasonal norm and that 2010 may get off to a slow start."

[Return to Top](#)

The College of Nanoscale Science and Engineering ("CNSE") presented its first-ever "Nano in the Mall" program on November 14, highlighting the role of nanotechnology in enabling energy efficiency and conservation. Led by Dr. Shadi Shahedipour-Sandvik, CNSE Associate Professor of Nanoengineering, and supported by a grant from the National Science Foundation ("NSF"), the event featured interactive demonstrations, displays and detailed information regarding alternative and renewable energy technologies.

Designed to engage members of the community on the importance of promoting energy efficiency and developing sustainable energy technologies, including new innovations in areas such as solid state lighting, the program gave visitors the opportunity to participate in hands-on activities involving LED lighting, as well as a up-close look at CNSE's research aimed at promoting clean energy technologies.



The event took place during CNSE's month-long community and educational outreach initiative known as NANOVember, part of the CNSE-KeyBank "NEXSTEP" initiative to promote greater understanding of the region's changing economic and business environment driven by nanotechnology, with a special emphasis on children, citizens and community.

[Return to Top](#)

For some time, analysts have been debating the possible growth of thin-film photovoltaics' popularity, with predictions taking various turns as the fallen price of polysilicon brings thin film's need into question. Although the contract price of polysilicon dropped by >50% last year, market analyst [iSuppli Corp](#) contends that thin-film solar remains a promising market.

Thin-film solar cells are quickly taking market share away from the predominant crystalline technology, according to iSuppli's latest report, with thin film's portion of PV wattage expected to more than double by 2013. Thin-film PV is expected to grow from its 14% in 2008 to 31% of the global solar panel market by 2013, in terms of watts.

The key game changer for thin-film prospects has been First Solar Inc. (Tempe, Ariz.), whose low-cost CdTe thin-film technology has taken off in the PV market. The company expects to produce >1 GW of thin-film panels in fiscal 2009.

"The market viability of thin

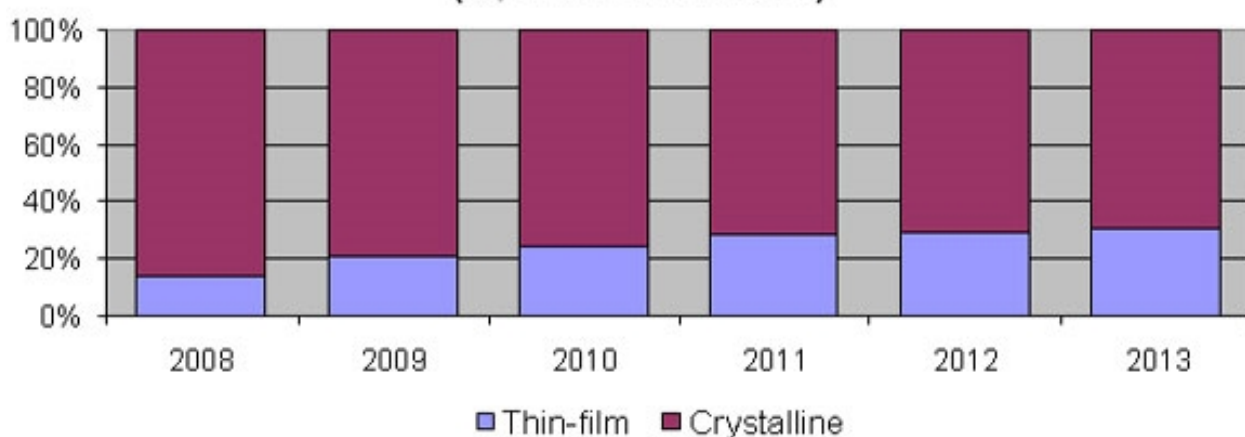
film has been solidly established by First Solar Inc. as it rockets to become the world's top solar panel maker this year, with more than a gigawatt of production," said Greg Sheppard, chief research officer for iSuppli. "At the same time, the company has driven its cost of production to less than 90 cents per watt, keeping its costs at approximately half the level of crystalline module producers."

The average thin-film solar panel price is expected to decline to \$1.40 in 2010, down 17.6% from \$1.70 this year. Meanwhile, average prices for crystalline panels are expected to drop to \$2 in 2010, down 20% from \$2.50 this year. Crystalline prices will continue to close the thin-film pricing gap through 2012, brought on by the dominant companies pouring on capital spending, technology R&D and manufacturing refinements, according to iSuppli. So while thin film's advantage has traditionally been its lower cost of production vs. crystalline's higher conversion efficiency, that is becoming less of a selling point.

Nonetheless, iSuppli expects thin film's place in the market to continue to grow, helped in part by the rising availability of turnkey production lines from companies such as Applied Materials, Oerlikon Solar and Centrotherm.

[Return to Top](#)

Thin-Film vs. Crystalline Solar Panel Production (%, in terms of watts)



SEMATECH engineers and the industry at large continue to make progress in developing the infrastructure that will enable lithography for cost-effective manufacturing, according to papers presented at the 2009 International EUVL (Extreme Ultraviolet Lithography) and 193 nm Immersion Extensions Symposia in Prague, Czech Republic. This year's symposia were co-organized by SEMATECH in cooperation with IMEC, Selete, EUVL, and EUVA. At the week-long duo of lithography events, an impressive attendance of nearly 400 top experts and researchers gathered to discuss progress on extending current technologies while building the infrastructure for future solutions. A combined set of 83 technical papers and 130 posters reported steady, measured progress in many key areas. At the same time, presenters highlighted various technology, infrastructure, and business challenges that the industry needs to address to successfully insert EUVL into manufacturing at the 22nm half-pitch node.

"While the economy is down, attendance was up this year and we surpassed last year's number of registrations," said Bryan Rice, director of lithography at SEMATECH. "I attribute this to a combination of the industry's critical need to address the cost and risk of developing EUV technologies and to a recognition that 22 nm solutions must be ready for insertion very soon – in 2013."

During this year's EUVL Symposium, steady progress was reported for EUVL including:

- * Experts from Cymer reported laser produced plasma (LPP) sources generate 50 watts at intermediate focus (IF). This compares with a system requirement of 180 watts needed to expose 100 wafers per-hour in high-volume manufacturing.

- * SEMATECH researchers and research partners highlighted the key role the consortium has played in achieving significant advances in EUV resists, specifically through achieving 20nm resist resolution images for chemically amplified resists and addressing the challenges of simultaneously meeting resolution, line edge roughness (LER), and sensitivity targets in a systematic way.

- * With EUVL moving closer to pilot line introduction, mask yield has become a critical focus and several chip manufacturers as well as consortia are using wafer printing and/or actinic aerial image review to characterize mask defects. Those printability studies show that the number of printing mask blank defects increases with decreasing feature size. About 50 percent of all inspected mask defects – mask blank defects, absorber defects, and pattern defects - print at the wafer level.

- * Lastly, the EUVL Symposium Steering Committee identified at the conclusion of the conference three remaining focus areas that the industry needs to work on to enable EUVL manufacturing insertion:

1. Availability of defect-free masks, throughout a mask lifecycle, and the need to address critical mask infrastructure tool gaps, specifically in the defect inspection and defect review area
2. Long-term source operation with 100 W at the IF and 5 megajoule per day
3. Simultaneous resist resolution, sensitivity, and LER

"Good progress has been made toward achieving resist resolution and sensitivity targets, with some improvement in line edge roughness, and now chip manufacturers are demonstrating post-exposure resist processes that lead to significantly reduced line edge roughness," said Stefan Wurm, EUVL Symposium co-chair and SEMATECH's associate director of Lithography. "With the world's leading-edge exposure tool for EUV resists learning, SEMATECH continues to enable the development of high performance resists required to demonstrate EUV manufacturability to our member companies and the industry."



Key progress indicators outlined at the Immersion Extensions Symposium, include the following:

- * Immersion lithography has been extended to the 22nm using a variety of approaches.
- * A wide variety of techniques including spacer, double etch, resist freezing processes, litho etch-litho etch, and source mask optimization were all demonstrated as viable double patterning approaches.
- * Invited speaker David Medeiros, of IBM, emphasized the explosion of masking at 22nm using double patterning in his presentation entitled "Lithography on the Edge." Sam Sivakumar of Intel predicted that future lithography processes will combine multiple approaches rather than a single winning technique in his presentation entitled "Technical and Manufacturing Challenges and the Prospect for HVM using ArF Pitch Division."
- * Although progress is being made towards enabling the 22nm node, the conference highlight was that the cost of ownership is of greater importance than the technical solution itself.

[Return to Top](#)

Casio Computer Co., Ltd. and Toppan Printing Co., Ltd. have agreed to form a joint venture to make organic light-emitting diode (OLED) displays. The company, as yet un-named, will be owned 80 percent by Toppan and 20 percent by Casio when it comes into being on April 1, 2010 and has the charter to research, develop, manufacture, and sell OLED displays and TFT LCDs.

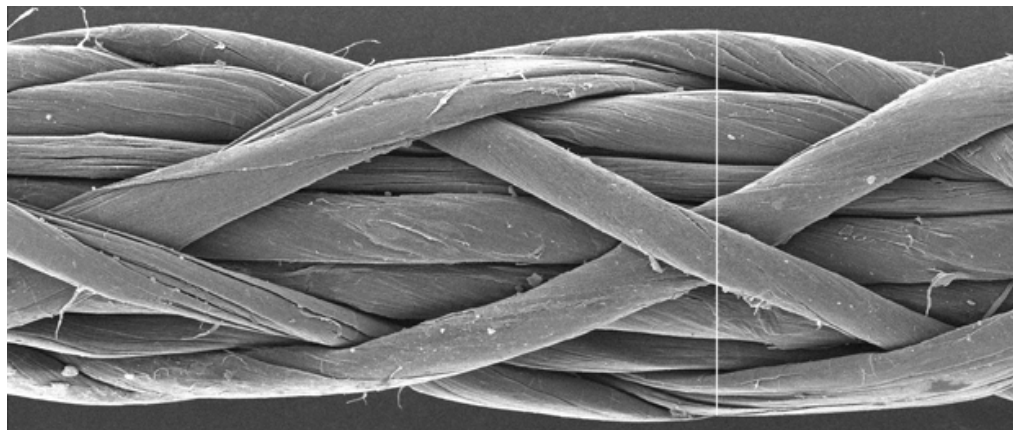
Casio will contribute its know-how and facilities related to small and medium-sized TFT LCDs. This technology is also relevant to the driving of OLED displays. Toppan will contribute fabrication technologies based on printing methods that Casio and Toppan Printing consider essential for the manufacture of OLED displays.

The company will be formed by Casio and encompass all the facilities and personnel in Casio's small and medium-size TFT LCD business and in OLED development. It will also take over ownership all shares in Casio's wholly owned subsidiary Kochi Casio Co., Ltd. Following that, 80 percent of the shares in the new company will be transferred from Casio to Toppan Printing on the target date of April 1, 2010.

[Return to Top](#)

Nanotech Product of the Week: ***Carbon Nanotube Sheets and Yarns by Nanocomp Technologies***

When carbon nanotubes entered the spotlight in 1991, visionaries and futurists had a field day. The structural, thermal, and electrical properties of these cylinder-shaped carbon molecules theoretically meant that, they could be used to build incredibly strong structures, such as a space elevator that would stretch 62,000 miles from Earth, or incredibly compact and fast digital computers. In practice, however, it has been tough to mass-produce nanotubes that are long enough for engineers to do any such amazing things. Now [Nanocomp Technologies](#), based in Concord, New Hampshire, is trying to bring the future closer by producing, in bulk, yarns and sheets made from carbon nanotubes.



On an atomic level, carbon nanotubes look like rolled-up tubes of chicken wire—only instead of metal, the tube is made from a hexagonal lattice of carbon atoms. Each tube is about one nanometer (one billionth of a meter) in diameter, hence the name. Today nanotubes are commonly produced in segments about 10,000 nanometers long, forming a black powder. This powder exhibits only a small fraction of the useful properties of nanotubes. Nanocomp says it can produce nanotubes that are tens to hundreds of times as long, forming carbon yarns and sheets (yarns up to one kilometer in length, with a tensile strength better than steel, and sheets made in 18-square-foot sections).

[Return to Top](#)

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