



COLLEGE OF NANOSCALE
SCIENCE & ENGINEERING
UNIVERSITY AT ALBANY State University of New York

Friday Morning Minutes

CNSE Weekly Newsletter

February 29, 2008

Today is Leap Day

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More than 30 scientific and technical papers based on research conducted at the College of Nanoscale Science and Engineering ("CNSE") of the University at Albany were presented this week at one of the world's leading conferences focused on the global nanoelectronics industry.

In all, 31 papers will be presented at the SPIE Advanced Lithography conference in San Jose, CA that represent work performed at CNSE's Albany NanoTech Complex either by CNSE research teams, by the CNSE global corporate partners' research teams resident at Albany NanoTech – including IBM, AMD, International SEMATECH, ASML, Tokyo Electron and Applied Materials – or by joint CNSE and partners' research teams resident at Albany NanoTech.

The papers cover a range of topics and outline innovative research in lithography, which is seen as critical to the manufacturing of future nanoelectronics devices. Included among the technical areas in which new developments are reported are extreme ultraviolet ("EUV") systems, resists and masks; immersion lithography materials and processes; and, optical microlithography.



Dr. Alain E. Kaloyeros, Vice President and Chief Administrative Officer of CNSE, said, "The presentation of more than 30 scientific and technical papers at the SPIE Advanced Lithography conference based on research performed at CNSE's Albany NanoTech Complex further demonstrates the world-class intellectual know-how and unmatched technical capabilities at the UAlbany NanoCollege. The recognized excellence of this truly unique resource for high-tech education, research, development and commercialization is a tribute to the vision, support and investment of New York's elected officials, which have created a pioneering educational paradigm at CNSE and accelerated technology development among the world's leading nanoelectronics companies."



Dr. James G. Ryan, Associate Vice President of Technology and Professor of Nanoscience at CNSE, said, "The scientific and technical papers generated at CNSE's Albany NanoTech by the NanoCollege and our global corporate partners underscore the power of collaboration between academia and industry in fostering innovation. We are confident that the developments reported at SPIE will play an important role in the effort to accelerate the introduction of extreme ultraviolet lithography into manufacturing."

The SPIE conference, being held February 24-29, attracts thousands of attendees and is considered the semiconductor lithography industry's most important technical event.

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Rudolph Technologies, Inc. (NASDAQ: RTEC), a leading provider of process characterization equipment and software for thin film measurement and macro defect inspection, and SEMATECH, the global consortium of leading chipmakers, have announced that Rudolph has become the first semiconductor equipment supplier company to join SEMATECH's Metrology Program headquartered at the College of Nanoscale Science and Engineering (CNSE) of the University at Albany. Under the membership agreement, Rudolph and SEMATECH will jointly establish an International Process Characterization (IPC) program, aimed at the development of process, analysis, and characterization technology to address critical challenges in nanoelectronics research. The IPC program, which will be a foundational component of SEMATECH's expanding metrology programs at CNSE's Albany NanoTech Complex, brings together expert researchers and technologists, along with critical tools and software, as part of the consortium's broader industry-university-government partnership with New York State and CNSE.

As the first associate member, Rudolph will team with SEMATECH's members and the members of ISMI (International SEMATECH Manufacturing Initiative) to accelerate the development and application of measurement methods for advanced semiconductor technologies. Rudolph's membership is the latest example of SEMATECH's new collaborative model, in which leading equipment and materials manufacturers can participate in focused, cooperative R&D with SEMATECH's members.



The IPC program will focus on integrated metrology, inspection and yield enhancement software solutions to address critical process characterization challenges identified in the ITRS roadmap for semiconductor manufacturing at the 32nm technology generation and beyond. The program will significantly benefit from the interactions among world-class researchers and engineers from Rudolph, SEMATECH and ISMI, and CNSE. "We are very excited to join SEMATECH in this groundbreaking research at the UAlbany NanoCollege," said Alex Oscilowski, Chief Operating Officer at Rudolph. "This is a truly unique opportunity for collaboration, with some of the best minds in the industry using a cutting-edge technology platform in the world's most advanced research complex."

Oscilowski outlined the difficult challenges faced by semiconductor manufacturers, including exponential growth in process complexity, decreasing size of systematic and extraneous defects, and increasing difficulty in discerning actionable information within the torrent of raw data. "The integration of advanced hardware and intelligent analytical software will be the key to meeting these challenges," he stated, "and we're looking forward to contributing our experience, front-end to back-end throughout the manufacturing process, and our broad expertise in metrology, inspection and data analysis technologies, to this important joint effort." [Read more from the Business Wire article . . .](#)

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Accretech Tokyo Seimitsu, a leading manufacturer of precision measuring and semiconductor manufacturing equipment, and SEMATECH, the global consortium of chip-makers, have announced that Accretech has become an associate member in SEMATECH's 3D Interconnect Program located at the College of Nanoscale Science and Engineering (CNSE) of the University at Albany.

SEMATECH's program is aimed at evolving the traditional copper/low-k interconnect technology to three-dimensional chip stacking, including through-silicon vias (TSVs) as interconnects. Launched two years ago, the 3D program has been recently opened to equipment and materials manufacturers, assembly and packaging companies, and others, in addition to SEMATECH's member companies. Accretech's membership is the latest example of this new collaborative model that encourages participation with SEMATECH members in focused, cooperative R&D.

Sadakatsu Suzuki, President and CEO of [Accretech](#), said, "As an equipment manufacturer, Accretech-Tokyo Seimitsu wants to contribute to the development and improvement of 3D chip and stack technology, working with the most advanced equipment and technology in the SEMATECH 3D Interconnect program." "We all recognize that collaboration among various disciplines across the industry will be required to realize

the full potential of 3D.

This is a perfect example of the evolution of the SEMATECH model where we are actively engaging with leading edge equipment and materials suppliers and leveraging their expertise to deliver manufacturable process solutions," said John Warlaumont, SEMATECH vice president of technology. "We look forward to working with Accretech to deliver the robust, manufacturable processes that will be key to our member companies' success in adopting 3D TSV technology."



Dr. James G. Ryan, Associate Vice President of Technology and Professor of Nanoscience at CNSE, said, "We are delighted to welcome Accretech Tokyo Seimitsu to the UAlbany NanoCollege, where it joins the fast-growing list of the world's leading high-tech companies engaged in cutting-edge nanoelectronics research at CNSE's Albany NanoTech Complex. This is further evidence that the vision and investment of New York's elected officials in supporting International SEMATECH's expansion at CNSE is paying dividends through world-class education and research, combined with economic outreach and growth."

"Being able to thin wafers uniformly with minimal damage and then handle the thinned wafers during subsequent processing are critical requirements for 3D processing," said Sitaram Arkalgud, SEMATECH's 3D program director. "Accretech is well known and respected throughout the semiconductor community for its expertise in the area of wafer thinning, handling and dicing, and their participation in SEMATECH's 3D program will be very valuable. We share the belief that 3D integration will be a key driver of chip performance and functionality, and working together we will accelerate progress toward industry-wide implementation."

3D interconnect technology requires bonding semiconductor wafers and/or dies and often uses deep through-silicon vias. The goal of SEMATECH's program at UAlbany NanoCollege is to enable high-volume manufacturing of 3D chips by its members with an optimum combination of cost, functionality, performance, and power consumption. When ready for volume manufacturing, 3D interconnects will provide cost-effective ways to integrate diverse CMOS technologies, and eventually link CMOS chips with emerging technologies such as micro- and nano- electromechanical systems (MEMS, NEMS) and bio-chips. [Read More at the CNSE web](#)

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Advanced Micro Devices Inc. says it wants to be able to break ground on its \$3.2 billion computer chip factory planned for Saratoga County by next January. AMD says it could even start pre-construction work on the 890,000-square-foot "chip fab" as early as July. That's what company officials told the Malta Town Board the past Monday night as it officially kicked off the public review process for the project, which calls for as many as three factories on Luther Forest Technology Campus in Malta built over many years. The company, based in Sunnyvale, Calif., also said the plant would employ 1,465 people - an increase from the original estimate of 1,200.

AMD has yet to officially commit to building at Luther Forest, but said it wants to have the necessary town site and environmental approvals in place so that it can have a building permit by the end of the year, should it decide to go forward. "It's a fairly lengthy process," said Terry Caudell, the company's director of wafer manufacturing strategies and project manager for what's being called Fab 4X. "Now is the time for us to work through these issues."

AMD actually has until the end of July 2009 to make up its mind about the plant and still be eligible for \$1.2 billion in state incentives. "We can't give that commitment tonight," Caudell said. But Caudell hinted that the company may be in a position to give more insight into its plans in the next several months. "We will do that just as soon as we can," Caudell said.

Any such announcement would likely come after an expected visit by Hector Ruiz, AMD's chief executive, to the area. Ruiz is planning to tour Luther Forest early next month. "There is no relationship in terms of an announcement," Caudell said when asked if Ruiz was coming here to officially commit to the project. Ruiz was last in the Capital Region in June 2006 when he announced the blockbuster deal to build the plant with

then-Gov. George Pataki at the University at Albany campus.

Meanwhile, the Town Board will have its hands full as AMD goes through the local regulatory process. Over the weekend, AMD submitted its plans to the Town Board in a hefty binder. As of last night, town officials were attempting to upload the documents to the town Web site so the public could look at them. AMD needs the Town Board to amend a law it passed back in 2004 that allows for Luther Forest to be developed for chip manufacturing. The amendments would allow for the specific needs of AMD, compared to generic needs originally set out in the law before AMD was a candidate to build on the site. For instance, the original law allows for four plants, while AMD wants to build just three that would be larger than originally envisioned. AMD is also submitting a supplemental environmental impact statement that must get town approval. The company was hoping for a public hearing on that as early as May.

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If you thought it was cool tying a video game to the physical world via consoles equipped with MEMS accelerometers, the technique Nintendo used to make "Wii" a household name, wait until you see what GPS can do to expand the future of video gaming. In an R&D project called [Mediascape](#), Hewlett Packard Labs, together with a team of U.K. researchers developed a location-based interactive software development platform. The goal is to link a collection of digital media fragments to the physical world using GPS, mobile devices and sensors. As a user with a GPS-enabled mobile phone or PDA walks, the device senses his position and triggers the appropriate media file.

By combining GPS and a digital compass with accelerometers, Mediascape lets gamers "become a mouse and a gamepad," said Patrick Goddi, a senior researcher at HP Labs. The R&D team is still in "an early phase of exploring the business model" for Mediascape, said Goddi, but the implications of the research are significant. First, it could define a new generation of video games that can be played in a "physical" or "mobile" environment-inside or out. Second, and perhaps more important, the new platform could serve as an engine for new social networking applications like blogging that are directly linked to physical locations. That fact could enable Mediascape to ride a growing GPS tidal wave in the mobile market.

If this year's Mobile World Congress was any indication, GPS is fast becoming more than a technology for car navigation. Nokia, Google and others increasingly view GPS as a key technology for defining a next-generation, "context-based" Internet. In rolling out its own Maps 2.0 service, Nokia's CEO Olli-Pekka Kallasvuo promised earlier this month that Nokia would take "navigation out of the car and bring it to the sidewalk." As a user snaps pictures with a camera phone, for example, Maps 2.0 could simultaneously store GPS coordinates in a metadata file, a capability known as geo-tagging.

HP's Mediascape platform would allow users, programmers and Web designers to go further. Using free Mediascape development tools and players released last year, some developers have already created several Mediascape programs, including a treasure hunt and a Yosemite National Park guide wiki-ed by forest rangers. Both programs linked a trail of clues or guide tips with location information.

Mediascape currently uses GPS to determine location, but the research team is planning to release support for Bluetooth beacons and other sensors so it can also work indoors.

HP's Bristol, U.K., group held Mediascape's first developers conference late last year, with more than 200 developers attending. While current Mediascape development is centered on games and education, HP hopes it can be applied to broader consumer and enterprise applications where information and media need to be associated with different locations.

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Nanotech Product of the Week: The Demron™ Full Body Suit by [Radiation Shield Technologies](#).

No wardrobe is complete without one of these hanging in your closet.

Radiation Shield Technologies (RST) is the sole producer of Demron™, a revolutionary lightweight, non-toxic, Lead-free, radiation protection fabric for individuals. Through a distinctive technology 8 years in the making, RST has perfected the development of this unique garment that can effectively shield the human body against ionizing radiation, while leaving its wearer unencumbered and fully mobile. Using a patented nanotechnology, Demron™ is currently manufactured into full body suits, blankets, tents, and other products to protect individuals during any radiological/nuclear emergency. Due to advanced molecular design, the Demron™ coverall allows for better heat dissipation than other impermeable protective fabrics, providing the user with a cooler core environment.



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